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IIEEJ International Conference on Image Electronics and Visual Computing 2024 Special Session: Industry Forum with APSIPA Industry Relations and Development, IEEE Signal Processing Society, IEEE Circuits and Systems Society, IEEE Solid-State Circuits Society

March 14, 2024, Afternoon (Taiwan Time GMT+8), Theme: AI and the Era of Smart Semiconductors

Motivation:

Niklaus Emil Wirth introduced the innovative concept of Programming = Algorithm + Data Structure. Inspired by this, we advance the concept to the next level by stating that Design = Algorithm + Architecture. As algorithms, especially those in Artificial Intelligence (AI), with high accuracy become exceedingly more complex and edge or Internet-of-Things generated data become increasingly larger, flexible parallel and reconfigurable processing are crucial in the design of lightweight systems with low complexity and low power. Furthermore, neuromorphic edge with non-von Neumann architectures witness broad applications such as in computing in memory (CIM), requiring energy-efficient design optimizations of the intelligent algorithm at the device level and possibly lower. Therefore, AI systems and smart semiconductor designs crossing levels of algorithm, system architecture, VLSI, circuit, device, etc. poses challenges which are key to the development and success of the global information technology and semiconductor community in the age of AI.

CHALLENGES BRING OPPORTUNITIES!

With these CHALLENGES amid current vibrant semiconductor environment, this Industry Forum (IF) provides a platform for experience sharing of new disruptive OPPORTUNITIES with yet more emphasis on AI and concurrent optimization of algorithm and architecture! This industry Forums targets students, young professionals & women-in-engineering (SYW). Industry speakers are invited to share pain spots or unmet needs with academia to innovate together for solutions. This provides students with real world research topics and/or possible internship opportunities. Academia work on real world problems with research outcome required by industry! As such this IF anticipates yet more emphasis on cross pollination between academia & industry in fostering Innovation, Internship, Industrialization, and Internationalization among Taiwan, Japan, and Korea!

Organizers:

Chris Gwo Giun Lee
Professor, National Cheng Kung University, Taiwan

Seishi Takamura
Professor, Hosei University; Visiting Senior Distinguished Scientist, NTT Corporation, Japan

Physical Conference in Taiwan & Virtual Connection with Everyone Else

Venue: F.C. Lecture Hall (繁城講堂) EE Department, NCKU

Free for all IEEE/APSIPA members

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Co-sponsors:
College of Electrical Engineering and Computer Science, NCKU
Academy of Innovative Semiconductor and Sustainable Manufacturing, NCKU
APSIPA Industry Relations and Development
IEEE Signal Processing Society, Tainan Chapter, IEEE CASS Society, Tainan Chapter, Taipei Chapter: IEEE Solid-State Circuits Society, Tainan Chapter

Program (13:20PM ~ 17:00PM)

(13:20 ~ 13:30) Opening Remarks: **Dr. Shoou-Jinn Chang**, Distinguished Professor *College of Electrical and Computer Engineering, NCKU, Taiwan*

- **Algorithm/Architecture Co-Design: From Algorithm to Architecture, and below...**

Session Chair: Professor Seishi Takamura, Hosei University, Visiting Senior Distinguished Scientist, NTT Corporation, Japan.

(13:30 ~ 14:00) Invited Talk: Dr. Keh-Jeng Chang*, Deputy Director, Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, Topic: SoC VLSI Physical Layouts and EDA Solutions to Enable Single-Digit Nanometer Semiconductor Volume Production for the Upcoming Artificial Intelligence.*

Distinguished Lecture Host: Prof. Kuang Wei Cheng, *Chapter Chair IEEE SSC Society, Tainan Chapter, National Cheng Kung University, Taiwan.*

(14:00 ~ 15:15) IEEE SSCS and CASS Tainan Chapter, Distinguished Lecture: Prof. Dongsuk Jeon*, Seoul National University, Korea, Topic: Designing a hardware solution for deep neural network training.*

(15:15 ~ 15:30) *Coffee Break*

(15:30 ~ 16:00) Invited Talk Dr. He Yuan Lin*, MediaTek, Taiwan,* Algorithm-Architecture Co-design for 4K HDR Video Applications in IC Design Industry.

(16:00 ~ 16:30) Invited Talk: Dr. Ryo Masumura*, NTT Corporation, Japan, Topic: MediaGnosis: Towards building multimodal foundation model.*

- **Panel Discussion: Emerging trends in Algorithm/Architecture Co-Design for AI & Young Professions, Students, Women-in Engineering in this New Era**

Panel Chair: Prof. Chris Gwo Giun Lee, National Cheng Kung University

(16:30 ~ 17:00) Panel Discussion:

Dr. Keh-Jeng Chang (TSMC), Prof. Dongsuk Jeon (SNU), Dr. He Yuan Lin, Eden Tsai (MediaTek)

Speaker's Information

Biography

Keh-Jeng Chang received the B.S. and M.S. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, and the Ph.D. degree in computer science from the University of California at Los Angeles, USA. After receiving his degree from UCLA, he spent more than 14 years conducting VLSI electronic design automation (EDA) researches in Silicon Valley in Northern California for two companies consecutively, i.e., Hewlett-Packard Company and Sequence Design Inc. Then, he returned to his home country Taiwan and continued his VLSI EDA researches at National Tsing Hua University and Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan. He has published scores of journal articles and conference papers and has been awarded more than 20 US patents, on methods and systems for yield improvement of nanometer CMOS and 3DIC.

Title

SoC VLSI Physical Layouts and EDA Solutions to Enable Single-Digit Nanometer Semiconductor Volume Production for the Upcoming Artificial Intelligence

Abstract

The continuous win-win collaborations among university scientists, circuit design houses, semiconductor chip manufacturers and EDA companies in the past decades will continue since world-wide semiconductor experts are postulating that the complexities of the upcoming high-end electronic systems and cloud and data center chip sets with generative artificial intelligence capabilities will soon be in the range of multiple trillion transistors. Majority of the transistors in the advanced systems are categorized as advanced nanometer CMOS transistors, such as FinFET and GAA/nanosheet. SoC VLSI physical layout innovations and EDA solutions in FinFET, nanosheet. and 3DIC alliance are believed to be essential to achieve the trillion-transistor trend within a few years. The leap from traditional SoC/IC designs to 3DFabric (3DIC) designs will bring new benefits and opportunities that come out of the legacy silicon CMOS. Furthermore, this new paradigm inevitably demands new solutions on system design, verification, thermal management, mechanical stress, and electrical-photonic compliance of the entire 3DIC assembly and reliability.

Speaker's Information

Biography

Dongsuk Jeon received a B.S. degree in electrical engineering from Seoul National University, Seoul, South Korea, in 2009 and a Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2014. From 2014 to 2015, he was a Post-doctoral Associate with the Massachusetts Institute of Technology, Cambridge, MA, USA. He is currently an Associate Professor with the Graduate School of Convergence Science and Technology, Seoul National University. His current research interests include hardware-oriented machine learning algorithms, hardware accelerators, and low-power circuits.
Dr. Jeon was a recipient of the Samsung Scholarship for Graduate Studies in 2009, the Samsung Humantech Thesis Contest Gold Award in 2021, and the Best Design Award at International Symposium on Low Power Electronics and Design (ISLPED) in 2021. He has served for the Technical Program Committee of the ACM/IEEE Design Automation Conference and IEEE/ACM Asia and South Pacific Design Automation Conference. He is now serving as a Distinguished Lecturer of the IEEE Solid-State Circuits Society and an Associate Editor of the IEEE Transactions on Very Large Scale Integration (VLSI) Systems.

Title

Designing a hardware solution for deep neural network training

Abstract

The size and complexity of recent deep learning models continue to increase exponentially, causing a serious amount of hardware overheads for training those models. Contrary to inference-only hardware, neural network training is very sensitive to computation errors; hence, training processors must support high-precision computation to avoid a large performance drop, severely limiting their processing efficiency. This talk will introduce a comprehensive design approach to arrive at an optimal training processor design. More specifically, the talk will discuss how we should make important design decisions for training processors in more depth, including i) hardware-friendly training algorithms, ii) optimal data formats, and iii) processor architecture for high precision and utilization.

Speaker's Information

Biography

He-Yuan Lin (林和源)
Senior Technical Manager
Platform System Architecture Div., Intelligent Software Development FU
MediaTek Inc.

He-Yuan Lin received his BSEE and PhD EE degrees from National Cheng Kung University. He has several years of research and development experience in IC design. His research spans algorithm/architecture co-design for visual processing. He currently serves as a senior technical manager in MediaTek's TV team, responsible for optimizing video codec development and related applications. MediaTek TV SoC business holds the world's highest market share and is recognized as a leading player in the industry.

Title

Algorithm/Architecture Co-design for 4K Video Applications in IC Design Industry

Abstract

Exploring the concept of algorithm/architecture co-design within the IC design industry, this presentation focuses on early algorithmic complexity analysis and joint optimization. Leveraging data flow and transaction level modeling, high bandwidth and IC area cost issues in 4K video applications are tackled. Through vertical integration of algorithms and architecture, this methodology enhances video application performance and cost-effectiveness, exemplifying its effective approach to real-world challenges.